Multi-Layer Memory Resiliency

Abstract:

With memories increasingly occupying a significant fraction of a chip’s real-estate, and the critical need to provision reliable, high-performance memory bandwidth for emerging applications, there is a need to build multi-layer hardware/software stacks that can adapt and opportunistically exploit manufacturing, operational and environmental variations in order to meet system performance/responsiveness, minimize power consumption, and increase system lifetime. The overall memory hierarchy is also highly vulnerable to the adverse effects of variability and operational stress.

This talk presents the concept of variability-aware memory management for nanoscale computing systems, building on the efforts of the NSF Variability Expeditions Project. After describing the challenges for dependability across the memory hierarchy, we show how to opportunistically exploit hardware variations in on-chip and off-chip memory at the system level through the deployment of variation-aware software stacks. Specific approaches to be presented include: hardware- and software-assisted memory virtualization for achieving dependable application execution; OS-level exploitation of DRAM power variation to save energy; incorporating heterogeneous memory organizations (e.g., SRAMs, Non-Volatile Memories) to increase dependability and enhance system objectives (e.g., performance, energy, system lifetime), and semantic retention of application intent to enhance dependability through exploitation of application semantics across multiple abstraction levels, including applications, compilers, run-time systems, and hardware platforms.

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Time: 1:30 o’clock p.m.
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