Guest Lecture
Dr. Dinesh PAMUNUWA
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Nanoelectromechanical Relay-Based Computing

Time: WED, 13th July, 2016, 11:00 a.m. – 12:00 p.m.
Location: CD0404, 4th floor, Gußhausstraße 27-29
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Abstract:

Digital circuits based on nanoelectromechanical (NEM) relays hold out the potential of providing an energy efficiency unachievable by conventional CMOS technology. Further, they can withstand much higher temperatures and absorbed radiation doses, offering ground-breaking improvements for harsh-environment operation. The main challenges are in achieving reliability over a sufficient number of hot switching cycles, miniaturisation and integration. These challenges are being addressed through innovations at the material, device architecture and circuit levels by different groups around the world. This talk will give an overview of the challenges and opportunities in NEM relay-based computing, drawing on experiences drawn from three multi-partner projects involving the University of Bristol, NEMIAC (EU grant 288670), NEMRAD (UK DSTL grant CDE38104) and NEMICA (UK Innovate grant 61931-453231).

Dinesh Pamunuwa (M’04–SM’09) received the B.Sc. degree (with honours) in Electrical and Electronic Engineering from the University of Peradeniya, Peradeniya, Sri Lanka in 1997, and the Ph.D. degree in Electronic System Design from the Royal Institute of Technology (KTH), Stockholm, Sweden, in 2003. He interned at the Berkeley Research Labs of Cadence Design Systems in Berkeley, CA during his PhD, working on timing and signal integrity analysis in integrated circuits. During this period he cofounded an electronics and software consultancy company based in Sweden and Sri Lanka. He was appointed to a Lectureship at Lancaster University in May 2004 and made a Senior Lecturer in 2010. He joined the Electrical and Electronic Engineering Department of the Merchant Venturers School of Engineering, University of Bristol as a Reader in Microelectronics on 1 Dec, 2011.

Dr. Pamunuwa has carried out research in the field of VLSI since 1999, focusing on the realisation of the next generation computing platforms for ultra-high performance and energy efficiency. The areas he has worked on include interconnect design and signal integrity issues, methodologies and architectures for electronic system design and networks-on-chip, architectures for nanoelectronics and nano-electro-mechanical (NEM) relay based circuit design.