

# Efficient Associative Processing with RTM-TCAMs

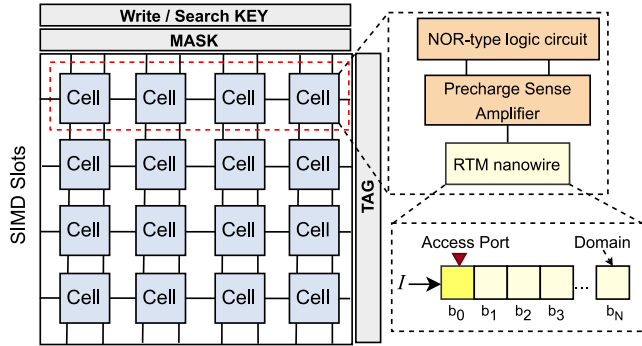
**João Paulo C. de Lima, Asif Ali Khan, Hamid Farzaneh, Jeronimo Castrillon**

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**Energy-efficiency in CIM approaches comes from reduced data-movement and massive parallelism**



**A + B**

Search 001-- Input pattern: A=0, B=0, Cin=1  
 Search 010-- Input pattern: A=0, B=1, Cin=0  
 Search 100-- Input pattern: A=1, B=0, Cin=0  
 Search 111-- Input pattern: A=1, B=1, Cin=1  
 Write ---1- Computation result: Sum=1  
 Search -11-- Input pattern: B=1, Cin=1  
 Search 11--- Input pattern: A=1, B=1  
 Search 1-1-- Input pattern: A=1, Cin=1  
 Write ----1 Computation result: Cout=1

*Associative Processors (APs) repurpose Content-Addressable Memories (CAMs) for SIMD tasks*

*No ADC/DAC*

*In-situ*

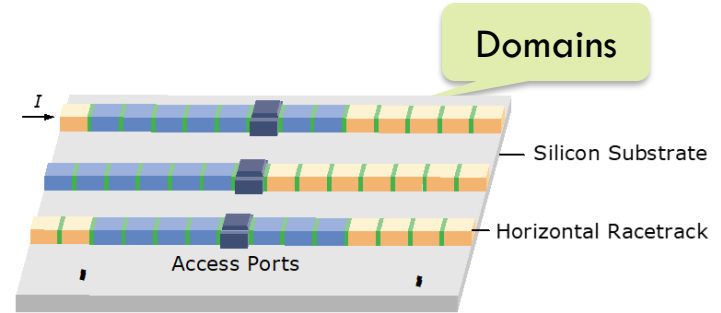
*Flexible types*

*Simple peripheral circuits*

# Why Racetrack Memories (RTMs) on APs?

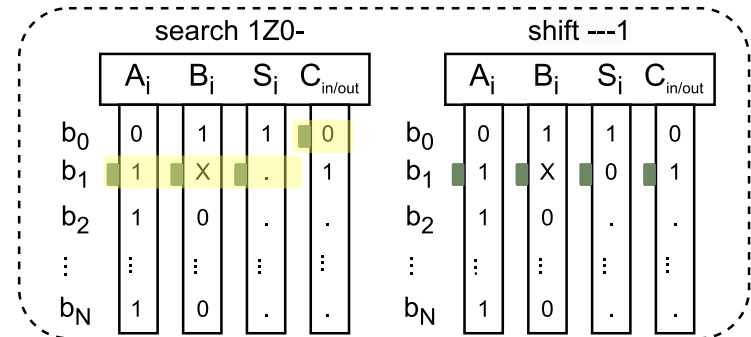
## 1. AP and multi-bit cells

- ❑ APs cannot profit from multi-bit capability in ReRAMs
- ❑ APs are bitwise by nature, similar to RTMs



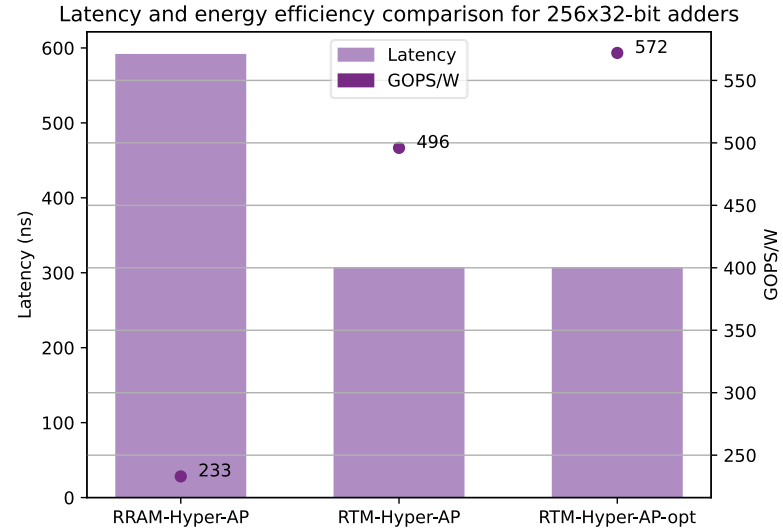
## 2. Write frequency

- ❑ Intermediate results, e.g., carry signal, need frequent writes
- ❑ RTMs' shift operation with pre-stored bits reduce the amount of writes



# Preliminary results

- RTM-AP exploits the inherent multi-bit RTM cells compared to other NVM-APs
- Reduced number of bits for Cin/Cout signals
- Write operations for Cin/out replaced by less-costly shift operations



*Reduced latency and improved energy-efficiency under iso-area comparison*